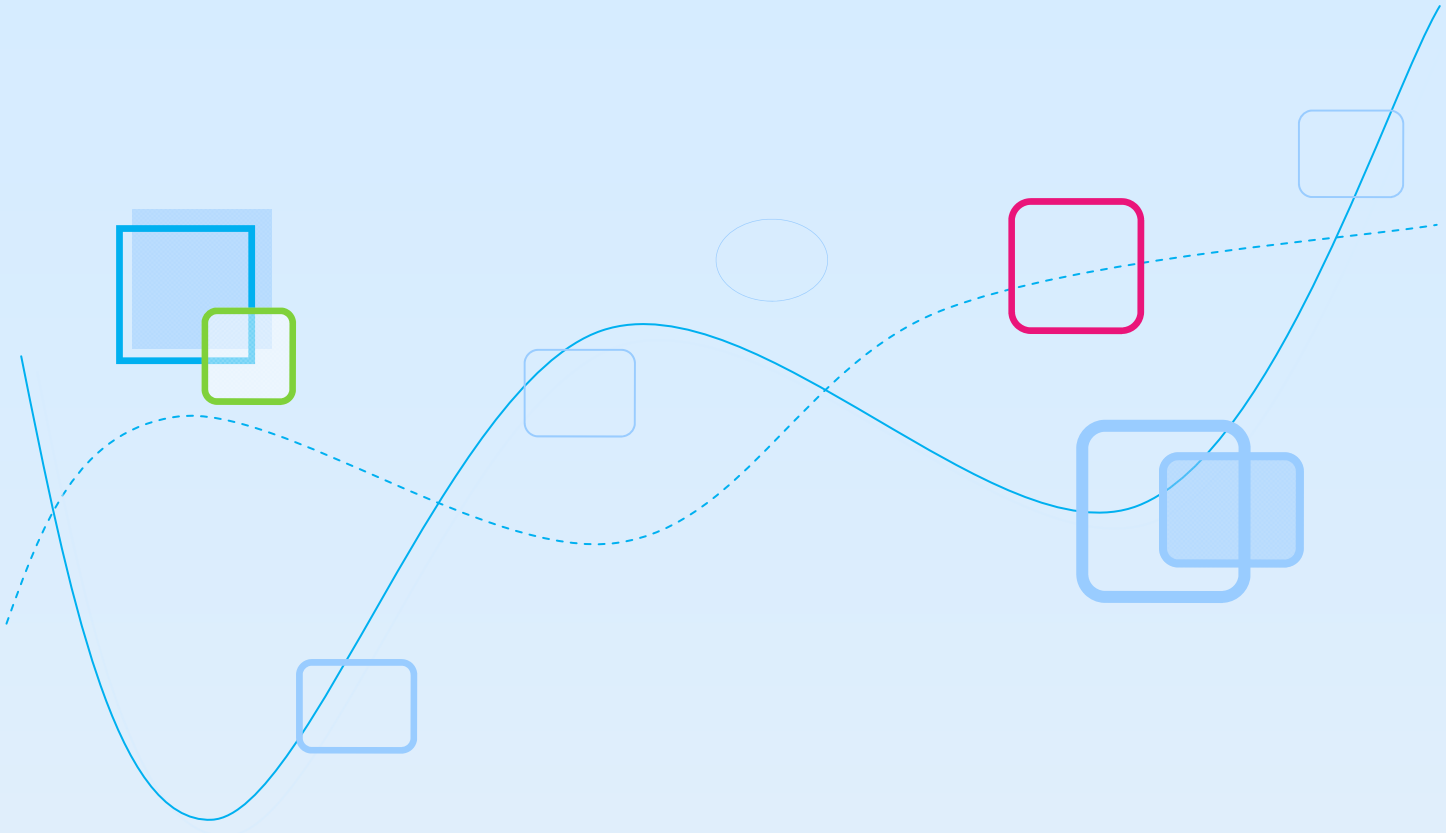


long Wavelength 320×256

Integrated Detector Dewar Cooler Assembly (IDDCA)

About this Document

This document contains the composition, specifications and performances of the long Wavelength 320×256 Integrated Detector Dewar and Cooler Assembly (hereinafter called LW 320×256 IDDCA).

Table of contents

1. Product Description

1.1. General description

The LW 320×256 IDDCA is an opto-electronic detector assembly that converts infrared radiation to detectable electronic signal. The responsive waveband is from 7.7μm to 9.5μm. IDDCA is composed of high sensibility long wavelength 320×256 Detector Dewar Assembly (DDA) and Stirling microcooler (Cooler), as shown in figure 1.

Figure 1: the photo of LW 320×256 IDDCA

1.2. The FPA

The core part of the IDDCA, the Focal Plane Array (FPA), is a pixel array with 256 rows and 320 columns. The pixel pitch is 30μm. As shown in figure 2, the imaging window can be flexibly chosen and the typical window and the size of the corresponding FPA are as follows:

- 320×256：9600μm×7680μm
- 320×240：9600μm×7200μm
- 256×256：7680μm×7680μm

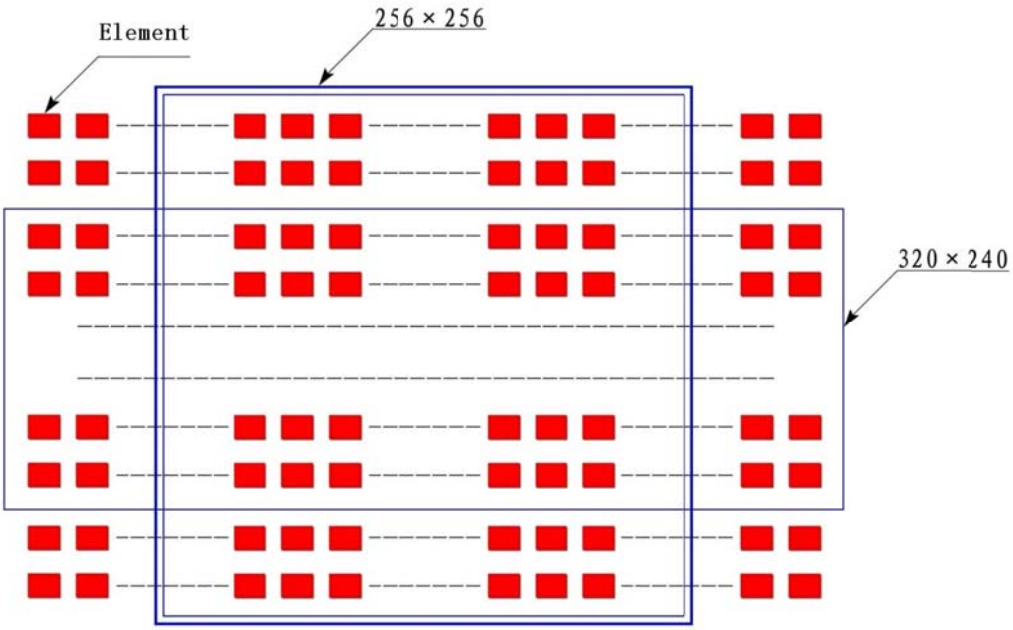


Figure 2: the diagram of the FPA

1.3. The ROIC (ROIC)

1.3.1. ROIC architecture

The design of the ROIC is based on the silicon CMOS technology. The ROIC architecture enables the FPA to integrate the information from the PV diodes (coupled by direct injection) simultaneously, then to store, to multiplex, to sample and hold the information

1.3.2. Operation mode

The design of the ROIC is based on snapshot operation with integrate then readout mode (ITR). The ROIC provides function including programmable integration time, selectable gain and number of output channels. With the same ROIC, three fixed array formats and one random windowing mode for subframe imaging are available.

1.3.3. Input stage

The design of the input stage is based on direct injection principle. Charges are stored in the input capacitance during integration time. The input stage has two gain options as shown in table 1.

Table 1: Gain options and corresponding capacitance

Gain level	Equivalent capacitance（pF）
0	0.7
1 (default)	2.1

1.3.4. Charge-Voltage (C-V) conversion

Charges are converted to voltages by C-V conversion circuit at the end of the integration. Each conversion is performed by amplifiers and controlled by the internal biases.

Four multiplexers (80 to 1) operate simultaneously to transfer the signal from amplifier to the four outputs. If the one output mode is selected, the four outputs are multiplexed in order to transfer the signals from the amplifier to the one output.

1.3.5. Output stages

The number of outputs is selectable between 1 output and 4 outputs using NBOUT input as shown in Table 2.

Table 2: NBOUT and the corresponding outputs

NBOUT	Number of Outputs
0	1
1 (default)	4

There are four output stages, i.e., one output stage for each multiplexer stage. The maximum output rate depends on the frequency range and the number of outputs selected, according to table 3.

Table 3: the maximum output rate of ROIC

	4 outputs mode	**1 output mode**
Frequency range 1	1-4 MHz (default)	1-6 MHz
Frequency range 2 (*)	5-8 MHz	7-10 MHz
*with proper bias voltage, the ROIC can be operated in frequency range 2， see paragraph ……。		

1.3.6. Sequencer

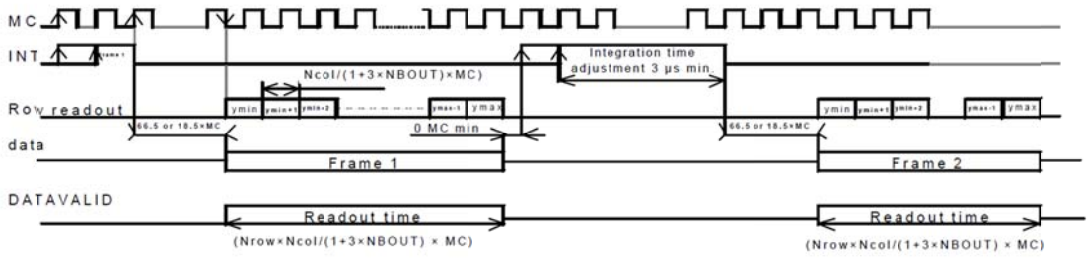


Figure 3: the sequencer of ROIC

The sequencer generates all internal signals necessary for the ROIC operation from the different external clocks and bias voltages. The ROIC operation is totally synchronous. All the pulses generated internally are multiple integers of the period of the master clock. A change in the master clock frequency induces a

change in these pulses. The clocks necessary to operate the sequencer are the master clock and the integration phase:

- Master Clock (MC) is the base for the synchronism of the operation of the whole circuit with a maximum frequency of 8MHz (125ns master period) and a duty cycle of 50 %. The pixel addressing is performed from static synchronous counters controlled by the master clock. The pixel information is read out at a rate of one per master clock period.
- Integration phase (INT) allows the integration of the charges in the pixel input capacitances (the PV diodes are biased during the high level of INT signal). The integration time is programmable continuously with minimum duration of 3 μs. The integration time, the duration of which is adjusted by moving the rising edge of the INT, should be multiple integers of the MC.
- The falling edge of INT corresponding to a rising edge of MC stops the integration phase by clamping the input MOS transistor.

The transfer of the first row to the charge-voltage conversion amplifier is performed during 66.5 master clock periods (except for the choice: 4 outputs 320×256 format and windowing mode where

the transfer is performed during 18.5 master clock periods).

Then, the DATAVALID output is set automatically at its high level. At the same time, the transfer of the second row to the charge-voltage conversion amplifier is performed. The DATAVALID signal goes down to its low level when all the pixels of the array or of the selected window are readout.

The minimum frame time is equal to the sum of the integration time and 18.5 or 66.5 master clock periods (according to the operational mode selection) and the readout time.

1.3.7. Format selection and windowing mode

1.3.7.1. Format selection

Three fixed formats and a windowing mode can be chosen thanks to SIZE-A and SIZE-B inputs. These SIZE-A and SIZE-B inputs allow to choose at each frame between the full window size (320×256, 320×240 or 256×256) and the reduced window defined through the serial interface.

As SIZE-A, SIZE-B and NBOUT have an immediate impact on the pixels to be integrated or on the digital part for the selection of pixels to be read, these inputs must only be changed between the falling edge of DATAVALID and the rising edge of INT.

SIZE-A	SIZE-B	Formats
1	1	320×256 (default)

1	0	320×240
0	1	256×256
0	0	Random windowing mode within 320×256

1.3.7.2. Window control and serial interface

In case of windowing mode, the size of the window selected is determined by the X and Y references of the corner points. The minimum size of the window is 64 columns × 1 row (within 320 columns × 256 rows). For the 1output mode, the possible width of the window is 64+n (0≤n≤256). And for the 4 output mode, the possible width of the window is 64+4×n (0≤ n ≤64).

Some rules apply on the coordinates to be entered in the serial data interface: the (X, Y) pixel coordinates can swing from (0, 0) for the first array pixel to (319, 255) for the last one (X = column, Y = row). The position of pixel (0, 0) = (column 1, row 1) relative to the dewar orientation is given in figure 4.

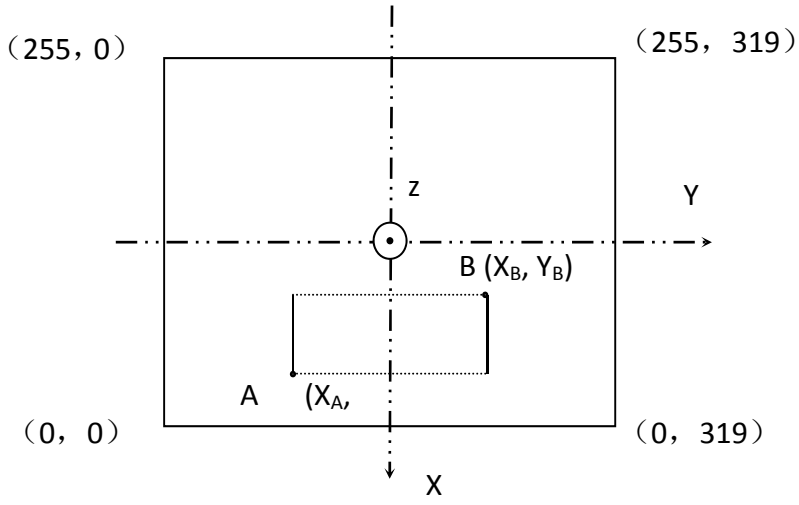


Figure 4: the relation between pixel coordinate and the dewar orientation

(X_A, Y_A) are the coordinates of the first corner of the window (point A), and (X_B, Y_B) the coordinates of the opposite corner (point B) and are addressed through the values X_{MIN}, Y_{MIN}, X_{MAX}, Y_{MAX}.

The pixels are addressed in the serial interface by block of 4 columns (one for each output) among 80. The Y coordinates are therefore independent of the output mode, but not the X coordinates.

$$Y_A = Y_{MIN} \text{ with } 0 \leq Y_{MIN} \leq 255$$

$$Y_B = Y_{MAX} \text{ with } Y_{MIN} \leq Y_{MAX} \leq 255$$

In the serial interface, Y_{MIN} and Y_{MAX} are therefore expressed with 8 bits.

For the one output mode, X_A and X_B are expressed as follows:

$$X_A = X_{MIN} \text{ with } X_{MIN} = 4 \times n, \text{ and } 0 \leq n \leq 64;$$

$$X_B = X_{MAX} \text{ with } X_{MIN} + 64 \leq X_{MAX} \leq 319;$$

Therefore, in the serial interface, X_{MIN} and X_{MAX} are expressed with 9 bits for the one output mode.

For the four output mode, X_A and X_B are expressed as follows:

$$X_A = 4 \times X_{MIN} \text{ with } 0 \leq X_{MIN} \leq 64;$$

$$X_B = 4 \times X_{MAX} - 1 \text{ with } (X_{MIN} + 16) \leq X_{MAX} \leq 80;$$

Therefore, in the serial interface, X_{MIN} and X_{MAX} are expressed with

7 bits for the four output mode.

The window coordinates data (X_{MIN}, Y_{MIN}, X_{MAX}, Y_{MAX}) are provided to the IRFPA through a serial interface consisting in the following inputs: SERCLK, SERCLR and SERDAT.

- SERCLK: clock of the serial interface with a maximum frequency of 10 MHz at 77 K. It allows the validation of the SERCLR and SERDAT inputs.
- SERCLR: allows the reset of the counter which controls the number of input bits. The number of bits is 34 for the one output mode or 30 for the four output mode. When it is not the case, the error bit (ERROR) is set at its high level indicating that the input data are incomplete or too numerous.
- At each window change, SERCLR must be set at the high level and validated by the SERCLK clock; then SERCLR must be set at the low level and the data bits must be entered.
- SERDAT: allows the input of serial interface data. Y_{MIN} (8 bits), Y_{MAX} (8 bits), X_{MIN} (7 or 9 bits) and X_{MAX} (7 or 9 bits) are entered in this specific order beginning with the maximum weight: [Y_{MIN} (7) ... X_{MAX} (0)], leading to 34 or 30 bits for the one or the four output mode.

1.3.7.3. Windowing function operation

The data necessary for the window definition (X_{MIN}, X_{MAX}, Y_{MIN} and Y_{MAX}) are put into the first register through the serial interface. If there is no error (ERROR at low level), these data are then put in the second register using parallel loading, between a falling edge of DATAVALID (thus at the end of an integration - readout cycle) and the next rising edge of INT.

When the ROIC is powered on, this second register using parallel loading is in an undetermined state. Thus, the following procedure must be followed in order to use the ROIC in the windowing mode:

- At the beginning of the power on of the ROIC, one fixed full format (320×256, 320×240 or 256×256) must be used for at least one frame. This ensures proper operation of the ROIC no matter what are the initial data of the parallel loading window registers ;
- The data of the first chosen window are sent through the serial interface ;
- When all the data are entered, the ERROR signal must be tested at the low level. If there has been an error during the data input (ERROR at high level after all bits input), the data must send again;
- After this verification, the data are sent automatically to the

parallel loading register during the falling edge of DATAVALID. Then, this register contains the valid data;

- The data defining the next window can then be sent at any time. They will be automatically applied, if there was no error in the transmission, at the end of a readout time, and will be valid for the next integration and readout cycles.

1.3.8. Dynamic range

Gain	Maximum storable charges in the ROIC	The corresponding maximum output
0	≥ 1.9 pC (12 Me-)	2.8V
1	≥ 5.9 pC (37 Me-)	

1.4. The dewar / cooler assembly

1.4.1. General description

The MW 320×256 IDDCA adopts highly reliable second generation dewar adapted with integrated stirling cooler as the cooling part.

1.4.2. Description of dewar

A sealed metal dewar is adopted for the IDDCA. To obtain a long vacuum life, the following methods are implemented: high reliable low leakage rate soldering, use of getter and a long duration high temperature exhausting process. A high efficiency cold shield system and temperature sensors at the level of the FPA are installed inside the dewar. The mechanical references are located on the cooler mounting flange. The electrical vacuum connector is

used for the dewar to achieve electrical output.

The subassemblies of the dewar are the cold plate, the dewar shell, the reusable electrically activated getter (maintains the vacuum lifetime of the dewar), the cold filter (a cold shield assembly to limit the field of view of the PV array and eliminate the unwanted incident radiation flux on the PV array), the optical filter, the cold finger which is the thermal interface between the cooler and the dewar, and etc.

1.4.3. Description of microcooler

The cooler, a micro cycle rotary stirling machine, together with the detector and dewar assembly (DDA), constitute the IDDCA. It provides an environment with lasting low operation temperature for the IDDCA.

2. Mechanical Interface

The mechanical description and the outline dimensions of the IDDCA are presented in the attachment B. All dimensions are given in millimeters at room temperature.

These mechanical interfaces are representative of the ordered product but modifications may happen after this document printing. Therefore precise customer system pre-design based on these drawings are not recommended. The guarantied interfaces are the ones delivered with the final product.

3. Thermal Interface

The IDDCA concept allows the reduction of thermal load therefore reduces power consumption of the cooler and enhances the operation reliability.

Two temperature sensors (2N2222 or resemblance) are located on the focal plane to monitor the FPA temperature. One of them enables the regulation of the cooler.

Care must be taken to reject heat generated by the compressor/motor assembly. Adequate heat sink and/or convective cooling shall be provided by the user to ensure that the surface temperature of the cooler body (compressor) does not exceed the ambient temperature by more than 10°C.

4. Optical Interface

4.1. General description

The optical interfaces consist of an antireflective coated infrared window, a cold filter, a cold shield and the infrared FPA. The optical interfaces are described in the Attachment C.

4.2. Infrared window and filter

The infrared window is antireflective coated in order to optimize the incident radiation on the PV array. It is made of Germanium (refractive index = 4) with a thickness of 1±0.05 mm. The cold filter is also made of Germanium (refractive index = 4) with a thickness of 0.3±0.05mm.

4.3. Infrared FPA

The focal plane is described in paragraph 1.2.

Due to the fact that the PV array is back side illuminated, the real position of the focal plane sensitive array is located inside the material.

The FPA position defined in the attachment corresponds to an equivalent air optical distance as if there was no cold filter and no CdTe substrate.

4.4. Cold shield

The cold shield allows the elimination of the unwanted incident radiation on the FPA. The aperture is aligned relative to the FPA.

The specific dimension of the cold shield refers to Attachment C.

5. Electrical Interface

5.1. Electrical interface of Infrared FPA

The electrical interfaces of the IRFPA are described hereafter.

5.1.1. Input interface

5.1.1.1. Introduction of the electrical interface

Refer to Attachment D for the detailed description of the electrical interface of the assembly. The adjustments of all inputs are defined by the value, the tolerance, i.e., the possible variation range without any performance degradation, the bias noise and the maximum current. The adjustments given in this document are valid for 5 V supplies. However, the system electronics shall have the possibility to adapt the supplies from 5V to 3.3 V, which may change other voltages levels. The bias voltage is given in the table below:

Electrical function name	Bias type	Range Value(V)	Typical value (V)	Tolerance (V)	Max. current (mA)	Max. noise ($nV/Hz^{1/2}$)
G_{pol} (PV diode bias)	Tunable	0 ~ 2	1±0.1	±0.005	< 1 (peak)	25
V_{DDA} (analog supply)	Fixed	5	5	±0.05	< 20	250
V_{DDL} (digital supply)	Fixed	5	5	±0.05	< 5	500
V_{SSA}	Fixe	Ground	0	-	-	-

(analog electrical ground)	d					
V_{SSL} (digital electrical ground)	Fixed	Ground	0	-	-	
SUB PV (PV diode substrat	Fixed	Ground	0	-	-	-
V_{GGAS}*	Fixed	1.2 ~ 1.5	1.35	±0.05	< 1	25
V_{REF}**	Fixed		internal			

*V_{GGAS}（Customization necessary）must be only used within frequency range2

**V_{REF} is internally generated, while it must be decoupled from the ground with a 100nF capacitance.

5.1.1.2. Biased Voltage

The bias voltages necessary to operate the CMOS processor are:

- One tunable external bias voltage which has to be adjusted from detector to detector to optimize the overall photodiode bias voltages (G_{POL});
- Two external bias voltages (power supplies V_{DDA} and V_{DDL});
- Three grounds (V_{SSA}, V_{SSL}, SUB PV).
- V_{REF} is an internal bias but must be decoupled externally from the ground by a 100 nF capacitance.

In case of operation in frequency range 2, at least one internal bias voltage (VGGAS) must be externally generated. In addition, seven fixed internal bias voltages can be externally generated when necessary.

5.1.1.3. Pulse Voltage

At least two pulsed voltages (MC and INT) are necessary to operate the sequencer of the CMOS processor. The step up and step down time of the MC should be less than 50ns. To diminish the jitter generated during integration, INT should be kept for 100ns during the low level voltage of the master clock. Besides these two pulsed voltages, seven other pulsed voltages can be used for optional modes as shown in the table below:

Pulse	Low level (V)		High level (V)	
	typical	required	Typical	Required
MC	0	< 0.6	5	> 2
INT	0	< 0.6	5	> 2
SIZE-A *	0	< 0.6	5	> 2
SIZE-B *	0	< 0.6	5	> 2
SERCLK *	0	< 0.6	5	> 2
SERCLR *	0	< 0.6	5	> 2
SERDAT *	0	< 0.6	5	> 2
GAIN *	0	< 0.6	5	> 2

NBOUT *	0	< 0.6	5	> 2

* Optional pulses

5.1.2. Output signal characteristic

The ROIC processor has two manners of output: 1 or 4 channels analog output (OUT or OUT1, OUT2, OUT3, OUT4), and two digital output (DATAVALI and ERROR).

The analog outputs can be charged up by an impedance R of 100 kΩ in parallel with a capacitance C of 10 pF (or 40pF for frequency no more than 4 MHz) external to the dewar. The signal output period is the master clock period. Thus the maximum output frequency depends on the operation frequency range of the CMOS processor.

Electrical function name	Typical low level (V)	Typical high level (V)
OUT1,OUT2,OUT3,OUT4	1.6 (0 current)	4.4 (saturated)
DATAVALID (Digital output)	0	5
ERROR (serial interface digital output)	0	5

The digital output DATAVALID on its high level indicates the presence of valid data on the analog outputs OUT_n. The digital output ERROR on its low level indicates the presence of valid data for the field reduction mode and is only used for this mode.

These digital outputs can be charged up by a resistance R of 10 kΩ in parallel with a capacitance C of 80 pF external to the dewar.

5.1.3. Power dissipation

The typical power dissipation of the ROIC is less than 80mW during frequency range 1 or less than 150mW during frequency range 2.

5.2. Minimum electrical interface

The standard conditions when the readout circuit is operated with the default mode (i.e. with the minimum electrical interface) are:

- Number of analog outputs : 4
- Format : 320×256
- Gain : 76.2 nV/e- (equivalent capacitance 2.1 pF)
- Output rate : 4 MHz.

In these conditions, the minimum electrical interface are one tuned bias voltage (G_{pol}), two power supplies (VDDL and VDDA), three grounds (VSSA, VSSL and SUBPV), two pulsed voltages (MC and INT); and the dewar mechanical ground.

5.3. Electrical interface of the temperature sensor

For each temperature sensor, the electrical interfaces are the sensor anode (pin DTA [+]) and the sensor cathode (pin DTK [-]).

5.4. Electrical interface of the microcooler

The assembly adopts XD-5B integrated Stirling cooler and the electrical interface of the cooler refers to Attachment A. The mechanical interface of the cooler refers to Attachment B.

6. Specifications and performances of the LW 320×256 IDDCA

Normally the IDDCA obtains a good performance when the temperature of FPA is not above 80 K. Refer to Table 1 for the general specifications and performances of the IDDCA. The practical specifications refer to the inspection report delivered with the final product.

Specifications and performances of IDDCA

Detector	
Pixel Pitch	30 μm
Spectral Response	(7.7 ~ 9.5) ± 0.3 μm
Responsivity	≥ 5×10^{7} V/W
Responsivity Ununiformity	≤7.0 %
NETD	≤20 mK (F/2 ,300K ,50% well fill, 50Hz)
Operability	≥ 99%
Weight	≤ 650 g
MTTF	≥ 6000 h
Storage Life	≥ 10 years
Environmental Adaptability	
Operation Temperature	-40℃～+65℃
Temperature Shock	-55℃～+71℃
Storage Temperature	-55℃～+71℃

7. Delivery

7.1. Content of delivery

- 1 set of IDDCA
- 1 short circuit loop
- 1 window cap
- 1 operation manual for each batch of product when delivering IDDCA
- 1 qualification certificate

7.2. Product Marks

There will be the following clear marks on the IDDCA:

- Product Model
- Serial Number
- Date of Manufacture
- Name of Manufacturer

7.3. Package

During the shipment, IDDCA is packed in anti-static bag which is put inside an anti-static plastic box.

8. Operation steps

1. Connect the detector and the driving circuit
2. Start the cooler to make the cold plate to reach working temperature of the detector.
3. Turn on the driving circuit, adjust the bias voltage of detector to the required value, and the component can work normally.

9. Attention

1. The short circuit loop must be installed when storing the component in case of static breakdown.
2. The assembly operation must be conducted on the anti-static workbench and the operator must wear anti-static wristband.
3. The window of dewar is coated with Ge film and easy to damage. The window cap must be put on when the component is not in use. Use lens paper to wipe the window.

10. Guarantee

The guarantee of this product is 12 months. This guarantee does not apply to damage resulting from abnormal use, misuse, abuse, neglect or accident.

If there is any problem, the user should contact the supplier for solutions.

Attachment A

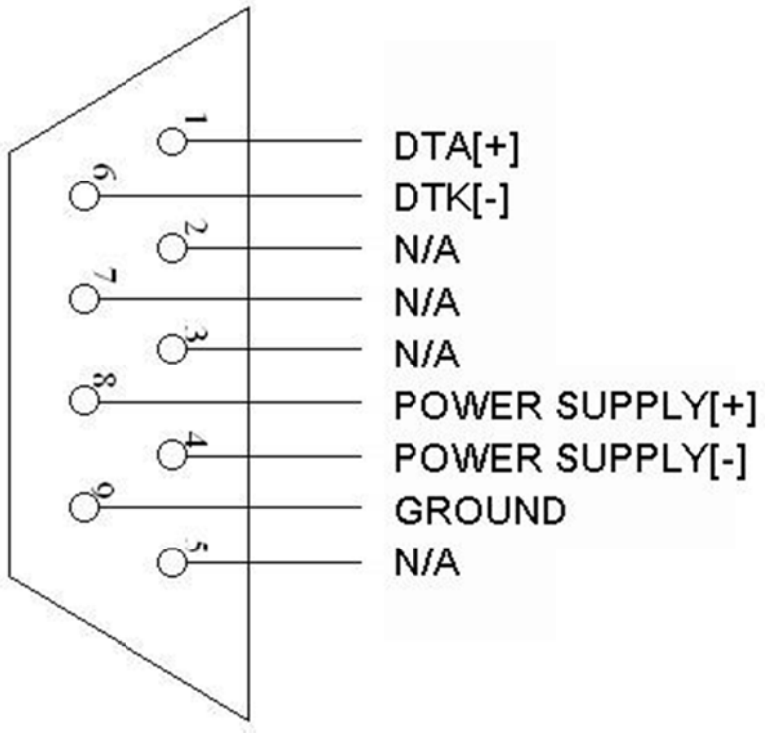
Instruction of the Cooler

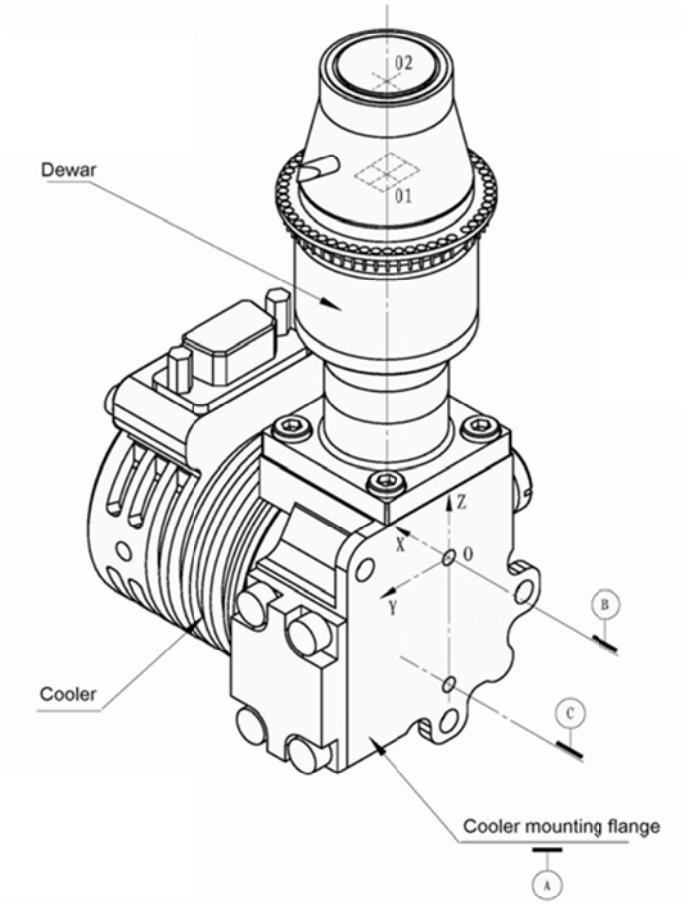
1 Power supply of the cooler: 24 VDC ± 0.5V

2 Maximum power consumption: 24 W

3 Temperature sensor voltage: 1.057 V ± 0.002V (1mA) @77K

4 The 9-way pin connector of the cooler electrical interface





Note

1、 Definition of the mechanical mounting references:

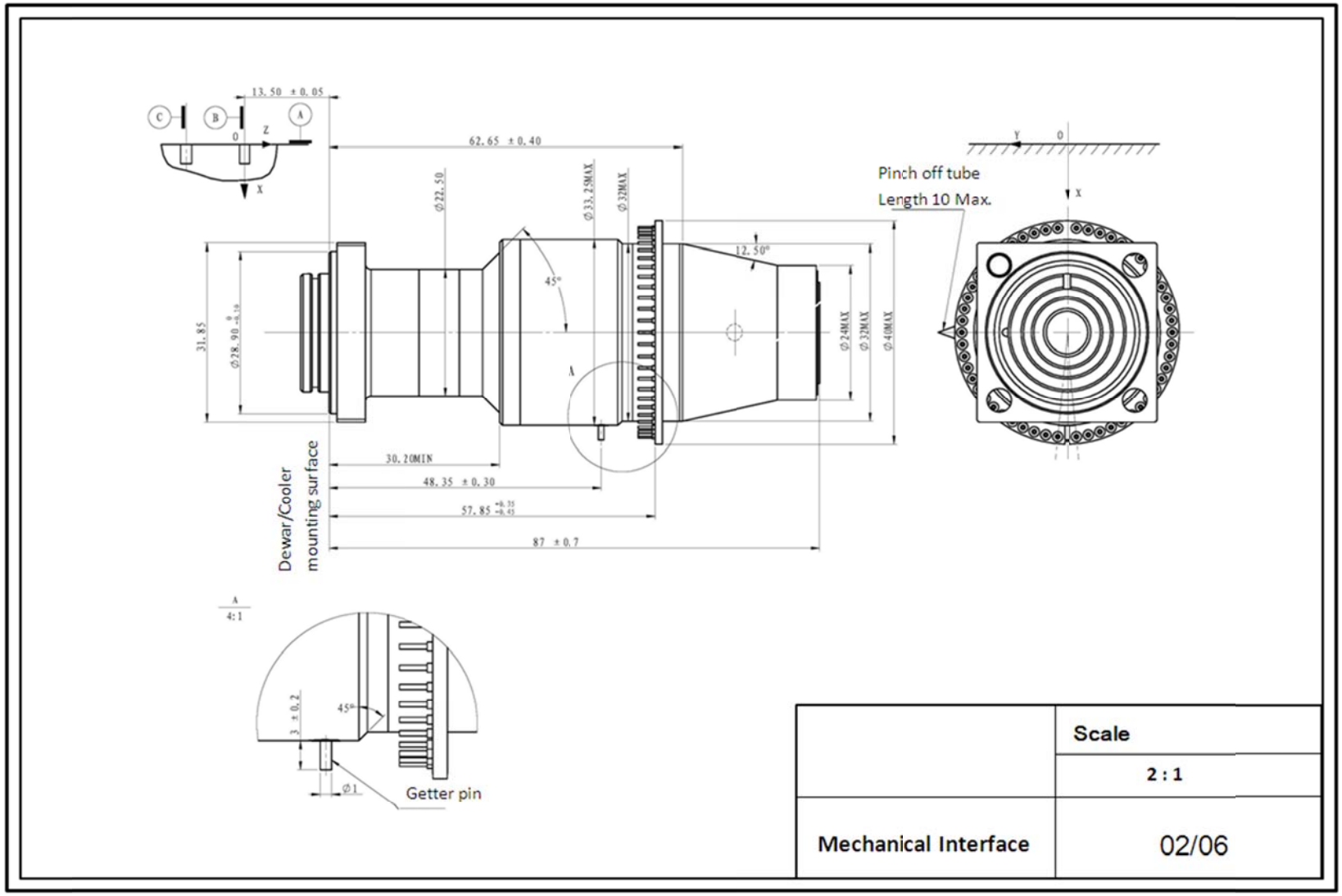
YZ: Plane of Cooler Mounting Flange
Z: Datum axis oriented by ϕB and ϕC centers
Y: Vertical to Axis Z on YZ plane, through ϕB center
X: Normal to YZ plane, through ϕB center
0: Center of ϕB on YZ plane

2、01 : Center of FPA

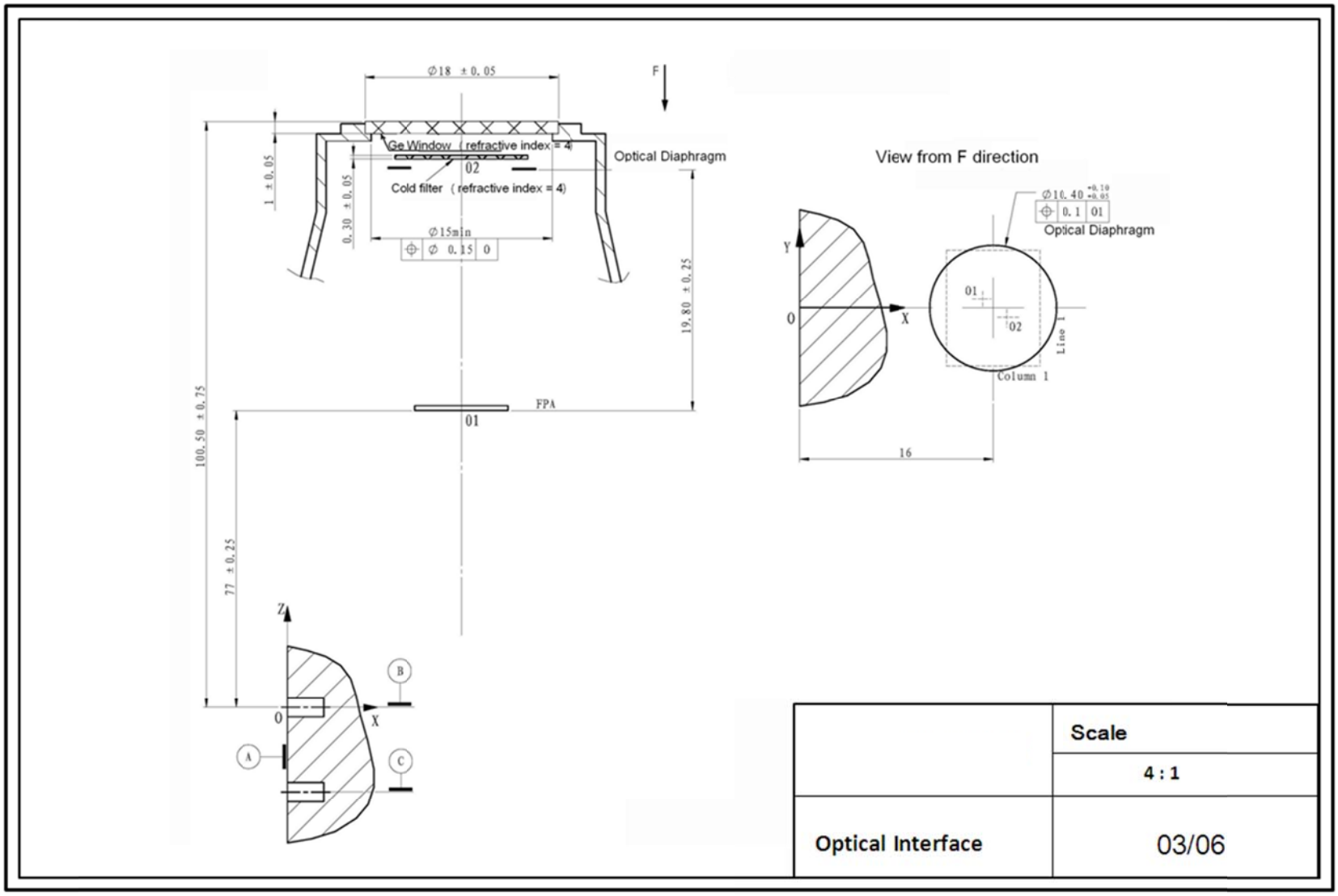
3、02 : Optical Center of Cold Shield

	Scale
	1.5 : 1
Mechanical Interface	01/06

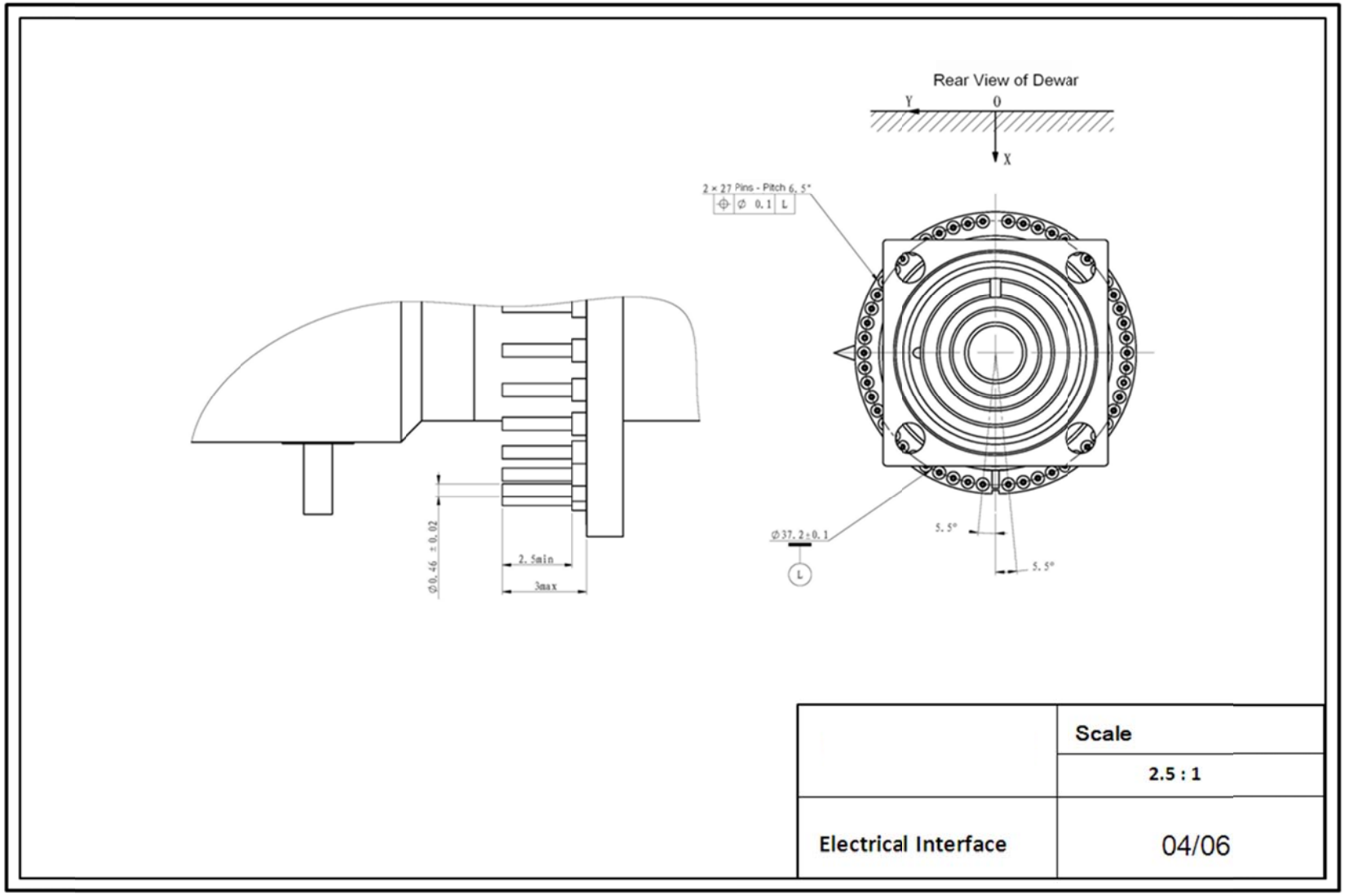
Attachment B-2



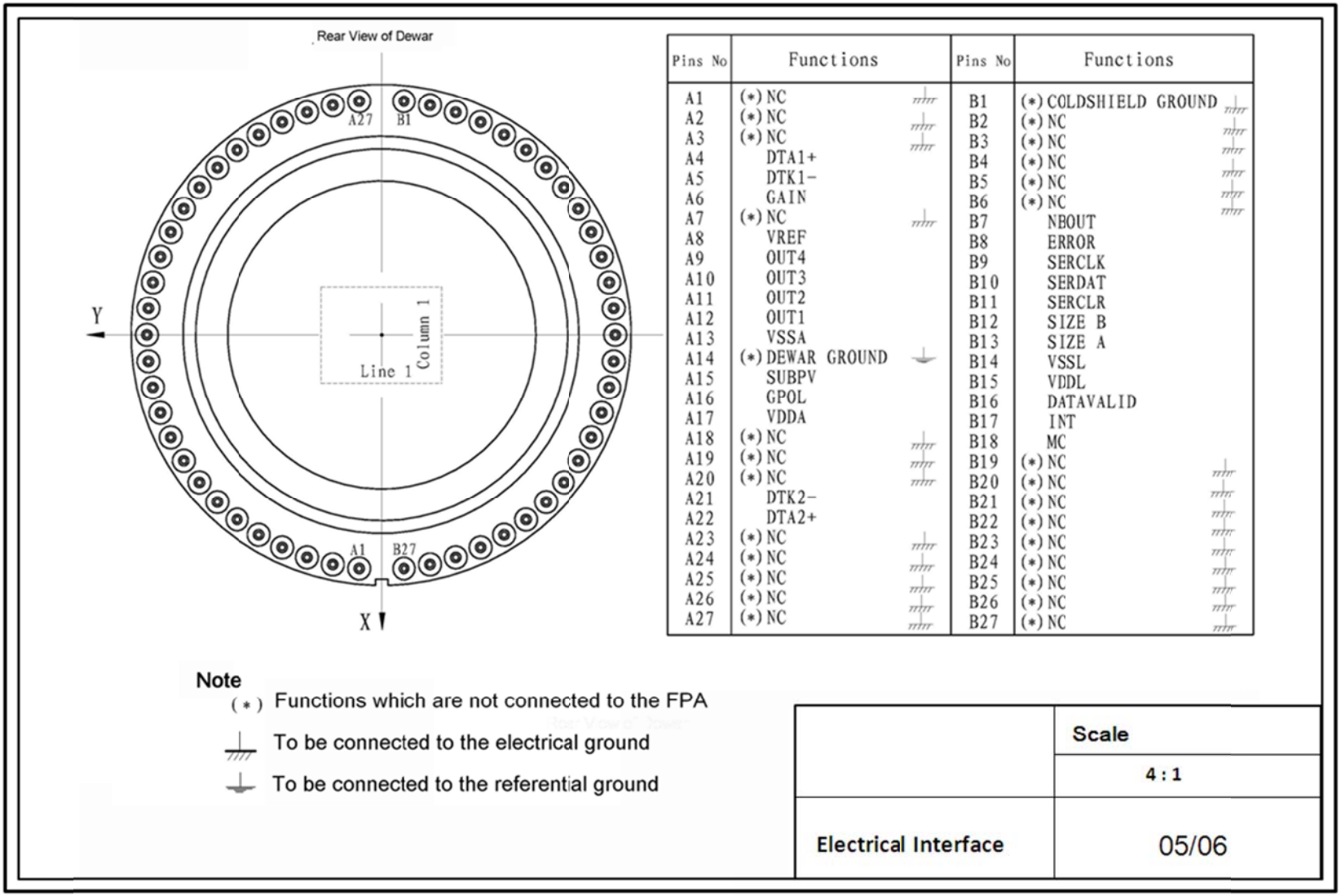
Attachment C (F/2)



Attachment D-1



Attachment D-2



Pins No	Functions	Pins No	Functions
A1	(*) NC	B1	(*) COLDSHIELD GROUND
A2	(*) NC	B2	(*) NC
A3	(*) NC	B3	(*) NC
A4	DTA1+	B4	(*) NC
A5	DTK1-	B5	(*) NC
A6	GAIN	B6	(*) NC
A7	(*) NC	B7	NBOUT
A8	VREF	B8	ERROR
A9	OUT4	B9	SERCLK
A10	OUT3	B10	SERDAT
A11	OUT2	B11	SERCLR
A12	OUT1	B12	SIZE B
A13	VSSA	B13	SIZE A
A14	(*) DEWAR GROUND	B14	VSSL
A15	SUBPV	B15	VDDL
A16	GPOL	B16	DATAVALID
A17	VDDA	B17	INT
A18	(*) NC	B18	MC
A19	(*) NC	B19	(*) NC
A20	(*) NC	B20	(*) NC
A21	DTK2-	B21	(*) NC
A22	DTA2+	B22	(*) NC
A23	(*) NC	B23	(*) NC
A24	(*) NC	B24	(*) NC
A25	(*) NC	B25	(*) NC
A26	(*) NC	B26	(*) NC
A27	(*) NC	B27	(*) NC

Note

(*) Functions which are not connected to the FPA

To be connected to the electrical ground

To be connected to the referential ground

	Scale
	4 : 1
Electrical Interface	05/06

Attachment D-3